Final Report

on

Advanced Motor Drives Studies

prepared for

NASA JOHNSON SPACE CENTER

Propulsion and Power Division

Power Branch

by

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Executive summary

This report gives an evaluation of advanced motor drives for space applications. The motor will drive a hydraulic pump system and will replace hydrazine fueled APU units. The motor drive must meet several requirements that are particular to space applications. Some of those requirements are small size, minimum loss rejection and high efficiency.

Soft-switching allows an increase in switching frequency and a reduction in inverter losses. Soft-switched inverters are therefore serious candidate for the replacement technology solicited by NASA. An efficiency comparison with the widely used conventional three-phase inverter backs up the case for this technology, which is gaining increased interest.

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1. Introduction

This report presents an evaluation of advanced motor drive systems as a replacement for the hydrazine fueled APU units. The replacement technology must meet several requirements which are particular to the space applications and the Orbiter in general. Some of these requirements are high efficiency, small size, high power density.

In the first part of the study several motors are compared, based on their characteristics and in light of the Orbiter requirements. The best candidate, the brushless DC is chosen because of its particularly good performance with regards to efficiency. Several power electronics drive technologies including the conventional three-phase hard switched and several soft-switched inverters are then presented.

In the last part of the study, a soft-switched inverter is analysed and compared to its conventional hard-switched counterpart. Optimal efficiency is a basic requirement for space applications and the soft-switched technology represents a unavoidable trend for the future.

2. *Statement of the Project*

NASA Johnson Space Center is interested in the evaluation of advanced motor drive systems that must meet the following requirements:

- Motor must deliver 40 hp in quiescent state and up to 140 hp peak power for short intervals of about 6 sec

- Drive will run a 3800 rpm hydraulic pump

- Weight of the motor drive system (motor & electronic drive) is not to exceed 91 lbs

- Drive will run from a stack of fuel cells whose voltage will vary from 27 V to 32 V. Nominal bus voltage is 128 VDC

- Efficiency of the drive must be > 90%, to minimize heat rejection and thermal management problem on board of the orbiter. The total weight of the three pump drive system, including the cooling should not exceed 2000 lbs.

These requirements have been made available to the Power Electronics Laboratory at Texas A&M University by NASA, JSC.

3. Motors

3.1. Selection Factors for Differentiating Various Motor Drives

Motor drives are selected based on several criteria. The priority of those criteria varies according to the specific application and resources involved. Some of those criterias are

- Cost

- Power Density

- Torque - to - inertia ratio

- Speed range and peak torque

- Losses and thermal capability

- Torque - per - unit current

- Braking

- Cogging and Ripple Torque

- Choice of feedback device

- Parameter sensitivity

3.2. Requirements on the motor

Electrical motors are usually designed to accomplish certain tasks. Usually the requirements of the load are specified in terms of speed and torque demands. A motor will have characteristics compatible to the load if it satisfies the speed and torque requirements of the load without exceeding the current limitation imposed either by the motor rating or the source capacity. Advances in power electronics allow almost any machine to have any other machine characteristics or any load requirement, given a fine tuned control of the system.

Furthermore a specific application and the environment may impose other constraints to the motor. The motor here should be designed for space restricted application. Space applications have severe limitations with respect to area or volume, weight. But thermal rejection must be minimal in order to minimize heat rejection system. For example machines having brushes like the DC motor are poor candidate for a space application. Basic requirements can be summarized as following

- High efficiency

- Minimum maintenance

- Rugedness

- High power density per weight and volume

3.3. Classification of DC and AC Motors

Electrical machines basically fall into 3 categories: DC motors, induction motors and synchronous motors. DC machines use DC current and come in different types while induction and synchronous machine use AC current.

3.3.1. AC Motors

3.3.1.1. Induction Motors

Induction motors are more widely used than all the rest of the electric motors put together. Before the emergence of power electronics they were mainly used in application requiring constant speed. Induction motors can be classified as following

- Single phase
  - * Capacitor
  - * Shaded Pole

- Polyphase
  - * Squirrel Cage
  - * Wound Rotor

3.3.1.2. Synchronous Motors

Synchronous machines have one particular characteristics: the speed can be precisely controlled by frequency control and made independent of variations in supply voltage, field current an load. They can be classified as following

- Sinewave
    - * PM
    - * Wound Field
- Brushless DC
- Hysterisis
- Step
    - * PM
        - * Hybrid
        - * Variable Reluctance
- Reluctance
    - * Switched Reluctance
    - * Synchronous Reluctance

3.3.2. DC Motors

DC motors are widely used in applications requiring adjustable speed, good speed regulation and frequent starting, braking and reversing. They can be classified as

* **Homopolar**

* **Commutator**
    - PM
    - Wound Field
        - * Shunt
        - * Compound
        - * Series
            - - Universal

3.4. DC Commutator Motors

DC motors are widely used in applications requiring adjustable speed, good speed regulation and frequent starting, braking and reversing. Basically 3 forms of DC motors exist: the separately excited DC motor where field and armature voltage are controlled independent of each other, the shunt motor where field and armature are connected to a common source and the series DC motor where field and armature current are the same. Although its control is very simple, it has some disadvantages.

3.4.1. Advantages

- Low Converter cost (few devices)
- Simple control
- No zero speed problem
- PM dc (Nd-Fe-B) machine can have considerable reduction in stator diameter
- Mature technology

3.4.2. Disadvantages

- Environmentally sensitive maintenance
- Limited speed, arcing between commutator segments
- Motor cost/size/weight
- Low terminal voltage due to mica insulation between the commutator segments
- Cooling difficult, poor termal path

3.5. AC Induction Motors

It is the most widely used motor in industry today. It is fed by AC current and exits in two basic forms: the simple squirrel-cage motor and the wound rotor motor.

3.5.1. Advantages

- Robust, reliable motor
- Motor cost/size/weight
- Environmentally insensitive
- No maintenance
- Lower cost in some applications
- Low inertia
- Able to operate at high temperature and high speed for long time
- higher efficiency than dc motors
- Available manufacturing infrastructure
- High horsepower, high voltage and high speed

3.5.2. Disadvantages

- Rotor losses, poor thermal path
- Complex control
- Power converter cost
- Control at zero speed
- Cooling is difficult, poor thermal path
- Additional power losses and torque pulsations due to the non-siussoidal voltage waveform of the converter.

3.6. *Switched Reluctance Motors*

The Switched Reluctance motor belongs to the class of synchronous motors. It has gone through steady and significant development over the last 2 decades. There are no windings or magnets on the rotor. The stator windings on diametrically opposite poles are connected in series to form one phase. Torque in a switched reluctance motor is developed by the tendency of the rotor to seek the minimum reluctance position which is the complete alignment of the rotor. By energizing consecutive stator phases in succession, it is possible to develop constant torque in either direction of rotation. Rotor position information is essential for the control of switched reluctance motors. The characteristics of the switched reluctance motor are summarized below:

- Torque produced by the tendency of the rotor to line up with the stator pole
- In motoring operation each phase is excited when its inductance is increasing
- Very robust and high speed operation possible
- High torque pulsation at low speed
- High switch volt-ampere rating
- High losses during field weakening region
- Both stator and rotor different from established technology
- High peak currents and high frequency can cause EMC problems

3.7. *Synchronous Reluctance Motor*

Synchronous reluctance motor drives have received renewed attention due to modern field oriented control strategies. A properly designed Synchronous Reluctance motor can perform as well as an induction motor narrow field weakening range. The stator of the synchronous reluctance machine is constructed from a structure identical to an induction machine. The rotor is usually designed purely for synchronous performance. A design for the highest reluctance difference is possible because damping winding is not necessary. Position sensor information is essential for field control of the Synchronous reluctance machine. Some other features of the Synchronous Reluctance motor are

- Conventional three phase stator windings

- Salient pole rotor to employ the principle of reluctance torque

- Lower torque and noise than Switched Reluctance Motor

- High saliencies for axially laminated steel rotor

- High rotor cost for axially laminated steel rotor

3.8. *Permanent Magnet Brushless DC Motors*

The Brushless DC motor is a synchronous motor having permanent magnets in the rotor instead of field windings. The excitation system does not include any brushes. Moreover the operation exhibits similarities with that of a dc motor. While the Brushless DC motor has the versatile control characteristics of a DC motor, it does not suffer from the limitations imposed by the commutator as restrictions on the maximum speed and power ratings, frequent maintenance and inability to operate in explosive and contaminated environments. Important features of the Brushless DC motor are summarized below.

3.8.1. *Features*

- Self synchronous motor with trapezoidal air-gap flux distribution and back EMF waveform
- Quasi-square wave armature current
- High number of poles reduces stator end winding overhangs and stator and rotor backirons
- Rotor available in the forms:
  - * Surface magnet
  - * Inset magnet
  - * Circumferentially magnetized
  - * Radially magnetized

3.8.2. Advantages

*   Constant torque operation

*   Constant power operation with field weakening up to a high speed
    due to reluctance torque

*   Higher reliability due to reluctance torque

*   Larger torque for the same peak current and voltage because
    of the interaction between rectangular magnetic field and
    rectangular current

*   Simple position detector such as Hall effect devices

*   Low inertia

*   No heat producing component on the rotor

*   High pole number reduces weight and material

*   Maintenance free

*   Control unaffected by variations in motor equivalent circuit parameters

3.8.3. Disadvantages

*   Rotor eddy current losses due to stator current harmonics

*   High cost of energy magnets

*   Magnet corrosion and demagnetization

*   Needs to be rated for higher power than IM for the same speed range

*   Higher stator current over field weakening region

3.9. Weight, Efficiency and Cost Comparisons

	Motor only	Motor + Drive
PM	100	200
SRM	150	250
IM	200	300
DC	400	450

Table 1 . Comparative weight (PM=100%)

	Motor only	Drive only	Motor + Drive
PM	97	93	90
SRM	94	90	85
IM	90	93	84
DC	80	98	78

Table 2 . Comparative efficiency

|	1993	1998	2003
DC	100	105	110
IM	100	90	80
SRM	150	90	70
PM	150	90	60

Table 3 . Comparative motor drive cost

The Brushless DC motor falls into the category of PM motors and has best results with respect to the criteria weight, efficiency and cost. Weight and efficiency are particularly important for space restricted applications. Predictions show that in the long run, the cost of a brushless DC drive will get cheaper. Although cost is not a major concern for this particular application, high quality at a cheap price certainly makes a stronger case for the brushless DC drive.

The Brushless DC drive is the clear winner. Power is supplied by fuel cells delivering dc current. The power electronics converter should therefore convert a dc current into a three phase ac. The inverters presented in the next sections include the conventional hard-switched three-phase and several soft-switched inverters.

4. Inverters

## 4.1. The Conventional Three-Phase Inverter
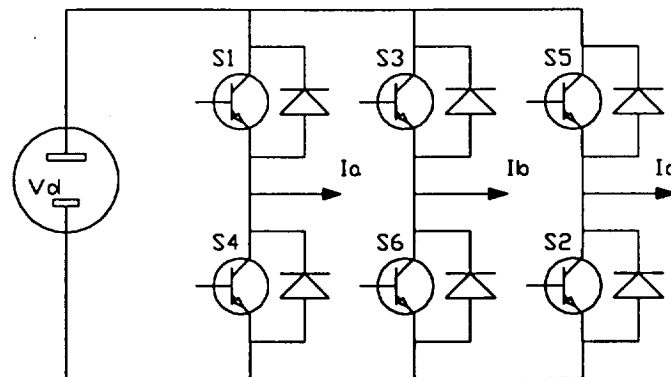
Fig. 1. Conventional Three-Phase Voltage Source Inverter

The conventional 3-Phase inverter uses 6 switches consisting of a turn-off power semiconductor and an antiparallel diode. Different PWM schemes are used to control the inverter:

*   carrier wave based PWM schemes

*   programmed PWM schemes

*   vector control schemes

All the techniques listed above operated under hard switched conditions, e.g. the switch are turned on and off at full bus voltage, thus generating high switching losses. During turn-on or turn-off, high voltage lies across the switch wherein high current flows in. The product of both yields the switching losses. This phenomena occurs at every turn-on and

turn-off. Switching losses are proportional to the switching frequency. Operation at high frequency would generate high switching losses and result in poor inverter efficiency. An upper switching frequency limit is usually set beyond which the inverter efficiency would become unsatisfactory for operation.
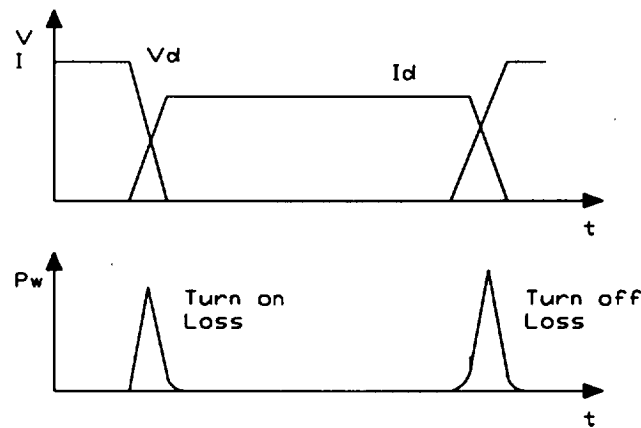
Fig. 2. Turn-on and off under hard switched conditions

Conventional hard-switched inverters are still widely used in the industry today. Hard-switched PWM operation is a mature technology and is the focus of numerous publications. Their potential is expected to rise given recent improvements in power semiconductor devices: switching times, power handling of devices, recovery behavior of diodes. Arguments for and against hard-switching are summarized in the next page.

4.1.1. Advantages of Hard-Switched Inverter

*   Simple power structure

*   Minimum VA rating of devices

*   Easy control

*   Low cost

4.1.2. Disadvantages of Hard-Switched Inverter

*   High peak stresses in devices due to inductive switching and reverse recovery of diode

*   Acoustic noise

*   Limitation on achievable switching frequency

*   Low power density

*   High $\dfrac{\partial v}{\partial t}$ which causes electromagnetic interference (EMI).

4.2. Soft Switched Inverters

Soft switching technique is widely used in the area of DC-DC converters and is finding its way into single or three-phase inverters. Basically soft switching is accomplished by turning devices on/off under conditions of zero voltage/current giving virtually zero switching losses. Soft switched inverters are broadly classified into two categories: Resonant Link Inverters and Resonant Pole Inverters.
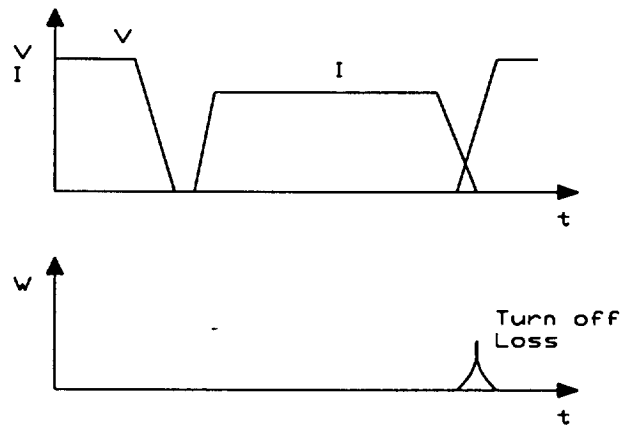

Fig. 3. Turn-on and off under soft switched conditions

Resonant Link Inverters are characterized by auxiliary circuits, typically including a resonant tank, which is placed on the dc side of the inverter. The dc bus, at the point of common connection, is made to oscillate such that possible commutation instant is set up for the inverter devices whenever the bus voltage (or current) reaches zero. Switching losses are thus reduced and high switching frequency are possible.

The Resonant Pole Inverter features one resonant commutation circuit per pole of the inverter which operates as to provide the desired resonant transition for the inverter. Here each phase can operate essentially independently from others and still provides soft-switching.

4.3. Resonant DC Link Inverters

4.3.1. Resonant DC Link (RDCLI)
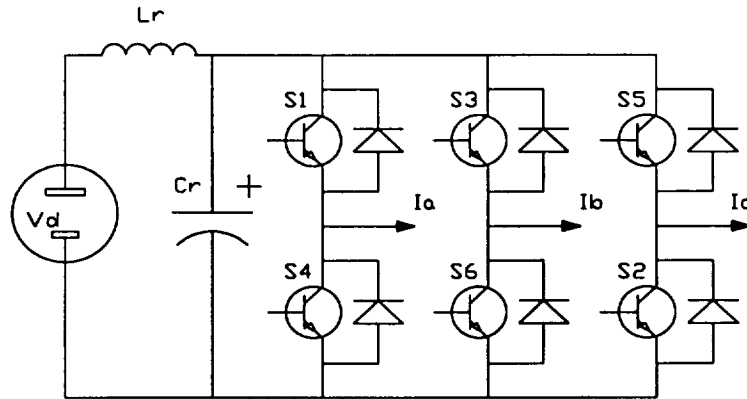
Fig. 4. Resonant DC Link Inverter

The resonant DC Link (RDCL), proposed by D. M. Divan of University of Wisconsin, Madison, was one of the earlier voltage source inverters circuits using soft switching technique. The circuit is similar to a conventional voltage source inverter with additional LC elements. The resonant elements set up an oscillation of the DC bus centered around the supply voltage. The link waveform oscillates between zero and $2V_d$ according to the formula [1]:

$$v_{cr}(t) = V_d \left(1 - \cos\omega_0 t\right)$$

with

$$\omega_0 = \frac{1}{\sqrt{L_r C_r}}$$

Therotically, the bus voltage v_{cr} has a peak value of twice the supply or link voltage V_d, but in practice, it can be higher, depending on the energy stored in the resonant inductor at the start of the resonant cycle

When the link voltage is zero volts, all the devices across the dc bus may be switched with no switching losses. During the zero volt interval of the bus, system losses are replenished through energy storage in the resonant inductor.

It is fundamental to size the LC components in relation to the load current/voltage. The circulating current may be a small fraction of the load current and still result in acceptable operation. The choice of the actual LC components is not obvious and depends on aspects such as loss minimization or other system optimization considerations. Clearly the choice of LC components determines the frequency of the link voltage and the sampling frequency of the control. The oscillating nature of the current and voltage waveforms provokes additional stresses, in the peak sense, to the devices. Devices should be rated higher if no clamp mechanism is integrated in the circuit. The voltage stress on devices could be $2.5V_d$ or higher. Different voltage clamp techniques are used to limit the peak voltage under $2V_d$. A clamp factor of 1.5 is typical.

Soft switching renders safe operating area limitations insignificant. This increases the maximum attainable frequency of the link and consequently the switching frequency. But the trade-offs in the design process of soft switched inverters are confusing and sometimes contradictory, since constraints and limits are different from those encountered in typical power electronics circuits.

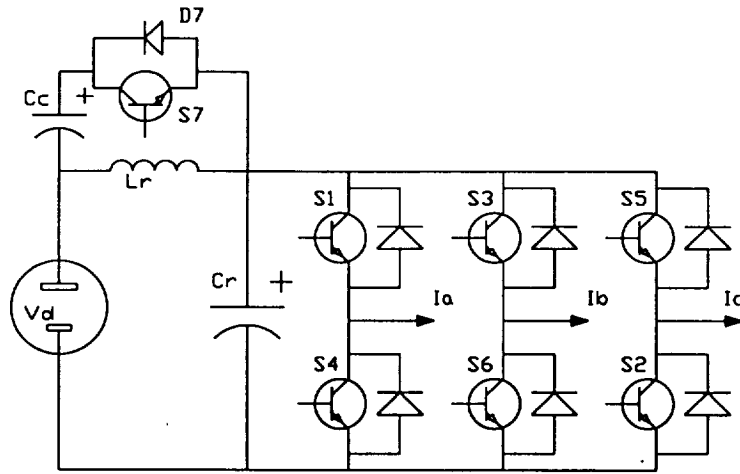*4.3.2. Passively Clamped Resonant DC Link (PCRDCLI)*
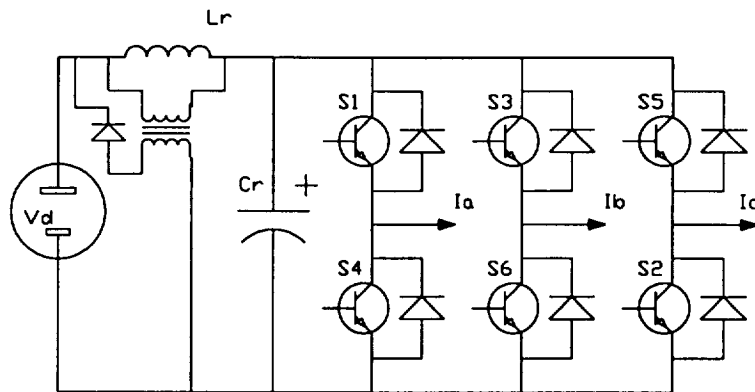
Fig. 5. Passively Clamped Resonant DC Link Inverter

The basic circuit is the same as the RDCLI. This circuit again is proposed by D. M. Divan and G.Skibinski. The passive clamp is implemented by a transformer connected on the primary side across the resonant inductor, on the secondary across the DC supply. A diode is connected in series with the secondary side of the transformer. The clamping level is set by the turn ratio of the transformer windings.

For a high Q LC circuit, the energy in the tank is conserved, except for the losses (in steady state). The resonant link is operated so as to compensate for these losses via control of the duration for which the bus is shorted. The clamping voltage must be greater than the steady state peak voltage stress of the devices. Sufficient energy must be stored in the inductor in order to ensure a return of the dc link to zero and establish the zero voltage condition. But limiting the peak voltage stress to a value under $2V_d$ would result in the removal of substantial energy from the resonant tank and the stop of the dc bus oscillation [2]. This is a drawback of passive clamping.

4.3.3. Actively Clamped Resonant DC Link Inverter (ACRDCLI)

Fig. 6. Actively Clamped Resonant DC Link Inverter

This circuit is proposed by D. M. Divan and G. Skibinski [2]. A seventh switched has been added to the basic topology of the RDCLI. The clamping voltage is not necessarily provided by an active source, but possibly by a precharged electrolytic capacitor. As with the RDCLI, the bus is shorted to allow precharging of the inductor current. On releasing the bus short, the link voltage resonates towards its natural peak. On reaching the voltage KV_d, diode D_7 turns on and clamps the bus voltage. With D_7 conducting, the switch S_7 is turned on in a lossless manner. The charge transferred to the capacitor with D_7 conducting is recovered when S_7 is turned on. When the net charge transfer is zero, S_7 is turned off and the circuit resonates until the bus voltage reaches zero.

The clamping voltage is usually greater than the supply or DC link voltage, and the topology is referred to as a Boost Clamp Resonant DC Link Inverter. An alternate actively clamped topology is possible where the bus voltage is clamped at the DC supply or DC link voltage. The average voltage of the bus is then lower than V_d. This is called the Buck Output Resonant DC Link Inverter.

4.3.3.1. Control of the Actively Clamped Resonant DC Link Inverter

One problem associated with the ACRDCLI or any RDCLI studied so far is that the bus has to be shorted for a precharging of the inductor current. One way to achieve this is to add a seven device across the dc link or to turn on all the main devices of the inverter for short time after each resonant cycle.

It is clear that the bus voltage become zero at discrete time interval kT_r, where T_r is the resonating period. Control of the inverter stage must be synchronized to the zero voltage duration of the DC Link, if zero voltage switching is desired. Consequently the inverter line-line voltage exhibits discrete pulses and a delta modulation type of strategy is suitable for inverter control. For voltage synthesis, a Sigma Delta Modulation ($\Sigma\Delta M$) strategy is indicated, while current control for ACRDCLI is best realized by Current Regulated Delta Modulators (CRΔM) [3].

Delta Modulators in control system are the family of uniformly sampled, zero-hysterisis, bang-bang controllers. A drawback of this control method is the existence of energy at subharmonics of the switching frequency, that degrades the spectral performance of the line-line output. In order for the control to be efficient, switching frequency should be high with respect to the output frequency of the inverter (a factor of at least 80 is minimum). One reason to select a discrete pulse over the conventional PWM is the much higher switching frequency. Results have shown that resonant link inverters switching at 3-4 times the frequency of hard-switched inverters yield approximately equivalent performance. 2 types of DPM regulators can be identified; the first essentially operates with computation and from existing values of feedback parameter while the second is computation intensive and requires direct feedback and estimation of system variables other than the parameter being regulated.

4.3.3.2. Characteristics of Discrete Pulse Modulation (DPM)

Switching under DPM operation does not occur randomly as under PWM, but at selected time intervals specified by a sampling frequency. In this case the link frequency must be an integer multiple of the link frequency, to ensure zero-voltage switching. Some characteristics of DPM are

* No equivalent to duty cycle

* Energy content exists at frequencies below link frequency

* Individual devices switch much slower than Flink

* Need to switch 3-4 times faster than PWM for equivalent performance

4.3.3.3. Voltage Synthesis
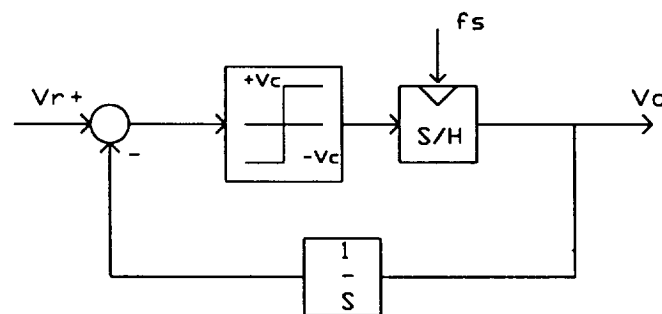
Fig. 7. Block Diagram of Voltage Regulator

Voltage regulation is achieved by ΣΔM. This is also referred to as an area comparison pulse density modulated regulator. The output voltage is fed back and the difference between the output voltage and the reference is integrated to provide the error function. This error serves as input of a block which has a function similar to a hysterisis regulator. The output of that block is sampled and initiates the switching of the devices. Particular attention should be given to the coefficient of the integrator in order to avoid clipping voltage which may cause the distortion of the desired output.

Voltage regulators are suitable for UPS applications since the quality of the output voltage is their most important specification.

4.3.3.4. Current Regulators
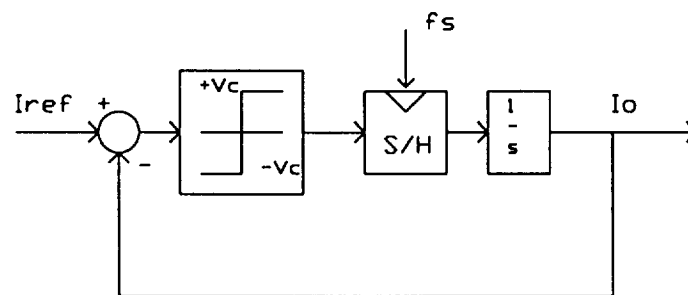
Fig. 8. Block Diagram for Current Regulator

In current regulators, current changes are governed by the load inductance (and resistance) as well as the load counter emf. The simple form of current regulator is the CRΔM, whose block diagram is shown in fig. 8. It is similar to the ΣΔM, with the exception that the integration is performed by the process itself. Loads in drive applications are inductive and contain an integrator. The only variable fed back is the current to be regulated.

Determining a selection strategy for the best set of switch inputs is very complex [4]. This can be done using a current vector. The current in the filter inductor at the next switching instant is predicted assuming that the output voltage is constant over the switching interval and that the resonant pulse may be replaced by a rectangular pulse with the same area. The actual direction of the resulting current vector is significantly influenced by the inverter voltage vector and is essentially a solution of the equation:

$$\Delta I_L = \frac{DT\ (V - E)}{L}$$

where ΔI_L is the current vector over the next switching cycle DT, V the inverter voltage vector, E the load back-emf and L the load transient reactance.

The CRΔM as described so far permits ± 1 transitions of any line-line voltage of the inverter. A modified version of the CRΔM is possible, that does not allow those transitions. It is referred to as the Adjacent State Current Regulator.

Ned Mohan and Bimal K. Bose have developed resonant DC Link inverters whose basic topology are similar to the ones presented earlier. They only differ in the clamping technique used to limit the bus peak voltage.

In the topology developed by Ned Mohan the peak bus voltage is clamped at the level of the DC supply or link. Furthermore one more degree of freedom is available since the width of a bus voltage pulse can be controlled independenlty. But it is also more complex and requires more devices.

4.4. The Pulse-Width Modulated Resonant DC Link Inverter

The Resonant DC Link inverter studied so far are controlled by discrete pulse modulation with the drawback of having subharmonics of the oscillating frequency. Random turn-on and off of the switches is not possible. A new strategy is being developed by D.M. Divan and Giri Venkataramanan [5]. The resonant capacitor is now distributed across each switch of the inverter. They are designed such that the equivalent capacitance across the bus still yields C_r. The active clamp circuit consisting of a switch and a clamp capacitor remains the same. In addition to the clamp function, it also assumes a control function.
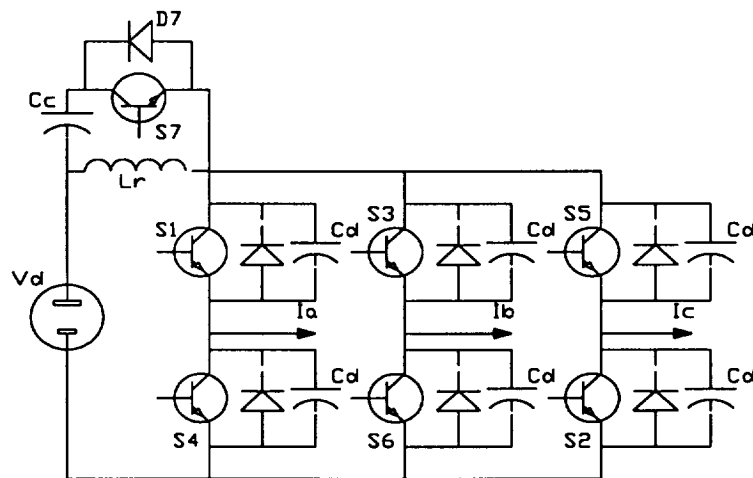

Fig. 9. PWM-RDCLI

One important feature of this circuit is that the inverter must be operated at the resonating frequency. The switch are turned on at the zero-volt interval of the dc bus and may be turned off at any time under zero voltage conditions, because a capacitor is connected across each switch. There is however a minimum on-time for the switch, which causes some restrictions to the PWM capabilities of this inverter.

Control of the PWM-RDCLI is done in a manner similar to the conventional hard switched PWM inverter. The carrier wave is sawthoot and not a triangle. The sawthoot frequency is the same as the link frequency. Using a sawthoot ensures that turn-on of the transistors is synchronized with the end of a resonant cycle. Turn-on occurs at zero-voltage at discrete time intervals of the link frequency. Turn-off occurs at any time during a resonant cycle and at zero-voltage because of the capacitor connected across each switch.

The long term objective is to emulate as nearly as possible the behavior of the conventional hard-switched inverter with all the advantages in the control and in the simple power structure, and still preserving the advantages of soft-switching such as minimal losses and high switching frequencies.

4.5. *Zero Current Voltage Source Inverter*

This inverter is proposed by H. Fujita, H. Akagi and M. Kohata. It has the resonating elements placed in series across each phase on the ac side. The $L_r C_r$ resonant tank is so designed such that the current in the switch goes through zero crossing. It is possible only if the resonating current peak is larger than the load current peak.
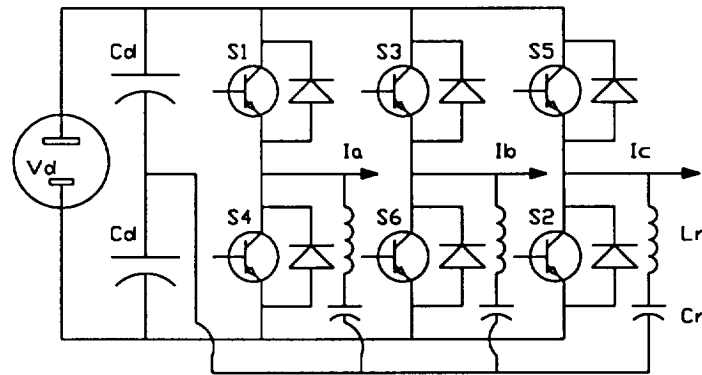
*Fig. 10. Zero Current Voltage Source Inverter*

The current flowing in a switching device is a sum of the load current and the resonant current. The switching device is controlled to be always turned on and off at zero current by regulating the amplitude of the resonant current. The amplitude of the resonant current in one phase can be controlled independently of other phases because the neutral point of the resonant circuits is connected to that of the dc link. The maximum frequency of the zero-current switching based inverter is half as high as the resonant frequency because a switching device can be turned on or off once a resonant cycle.

4.6. The Resonant Pole Inverter

4.6.1. The Resonant Pole Concept

The resonant pole is a basic concept that has been used in nearly all zero-voltage soft switching and resonant converters. The resonant pole consists of the main power devices paralleled with resonant capacitors. Compared with the conventional passive snubber circuit, the resonant pole has only turn-off snubbers. Turn-on snubber has to be provided by external means.

In resonant pole, it is crucial that the main devices are never turned on when voltage remains across the devices. It is necessary to reverse the sign of the pole output current after a resonant transition such that the resonant pole can change state from diode conduction to main device conduction. R. W. De Doncker proposes the following circuit for a RPI phase leg.
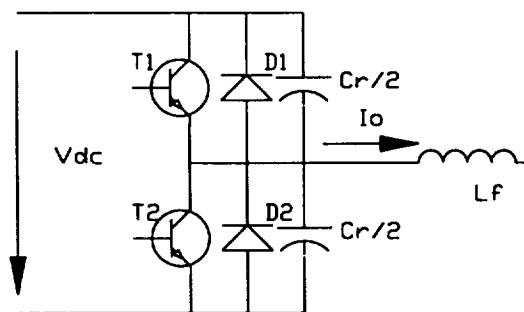
Fig. 11. Resonant Pole Inverter Phase Leg

4.6.2. The Resonant Pole Inverter

The Resonant Pole Inverter has the feature of integrating the auxiliary components together with output filter components. The load is connected at the center connection of the DC bus capacitors. The topology of the RPI is very attractive in power supply which require filtered output voltage waveforms, such as uninteruptable power supplies (UPS) and variable speed to constant frequency converters.

The instantaneous switching frequency of the RPI is dependent of the load current, the output voltage and the value of resonant components. The switching frequency varies dynamically during the output cycle. It is maximum at no load with zero output voltage and minimum at full load with maximum output voltage. If the switching frequency is much larger than the ouput frequency, then a filtered voltage waveform will appear across the output filter capacitors because Volt-sec balance has to be maintained across the resonant inductor [6].

Auxiliary circuit can be added to the basic topology of thre Resonant Pole Inverter to form the Auxiliary Resonant Pole Inverter and the Auxiliary Resonant Commutated Pole Inverter. Those new topologies have been developed by R. W. De Doncker out of the concern to reduce the conduction losses in the inductor and the power devices. Furthermore the new topologies remove the constrait of designing a sufficient low resonant impedance.

5. *The Resonant DC Link Inverter for the Brushless DC Motor*

The conventional hard-switched 3-phase PWM inverter is a mature technology. It is the standard in AC drives. Its control techniques have been investigated in numerous literature. Soft-switching on the contrary is relatively new for inverter although the technique has been used for quite a while in the area of DC-DC converters.

The choice of a Resonant DC Link inverter is justified if an increase in switching frequency is desired. For a conventional inverter switching at 5 kH, the soft-switched counterpart must be operated at around 20 kHz, in order to make full use of the advantages of soft-switching. Such frequencies are possible with IGBT (Insulated Gate Bipolar Transistor) in the medium power range.

In space applications, energy is usually supplied by a stack of fuel cells. In this particular case a stack of 5 cells deliver a total voltage of 128 VDC, which is considered the nominal bus voltage. The inverter must deliver 40 hp in quiescent state and up to 110 hp peak power for intervals of about 6 sec. In order to have those requirements met, the supply should be able to deliver high current and the devices capable of sustaining them. Of the devices used are not rated for those high currents, they should be connected in parallel.

The Brushless DC motor with trapezoidal back-emf has only 2 phases excited at any time. For constant torque, stator current must be square wave. The third phase is unexcited. Fig 12 shows waveforms for ideal operation of the brushless DC motor.
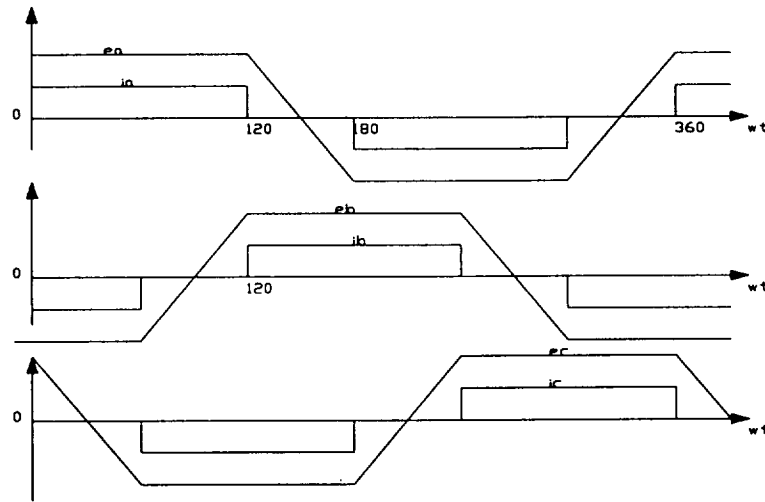
Fig 12 . Phase currents and back-emf of brushless dc

A three phase star connected design is chosen. Two of the three phase are active at all times and each phase is commutated every sixty electrical degrees. The power supply works like six four-quadrant choppers for one cycle. There is a zone defined between two commutations, which corresponds to six zones for one cycle.

5.1. Analysis

When 2 transistors are on (an upper and a lower), current flows from the supply to the load and the circuit can be simplified to fig 13.
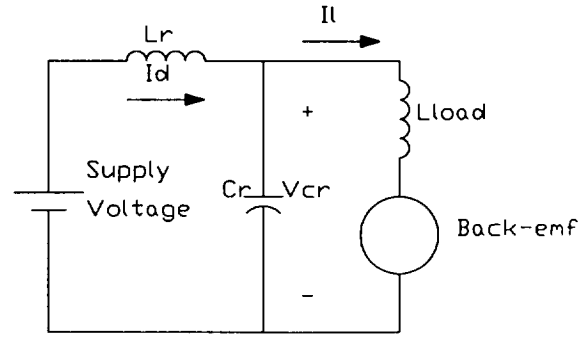
Fig 13 . Equivalent circuit for 2 transistors on

The circuit equations are then:

$$d - u_{cr} - L_r \frac{\partial}{\partial t} i_d = 0$$

$$u_{cr} = 2 L_m \frac{\partial}{\partial t} i_L + E_{LL}$$

$$i_d = i_r + i_L$$

$$i_r = C_r \frac{\partial}{\partial t} u_{cr}$$

where

V_d	: DC supply voltage	L_r	: resonant inductance
L_m	: machine inductance	E_{LL}	: phase back-emf
i_d	: input current	i_L	: load current
i_r	: capacitor (resonant) current	C_r	: resonant capacitor

When a switch is turned off (in this case a lower switch), the load current freewheels through a diode (here a upper diode) and all the input current flows through the resonant capacitor. After some substitutions, the following differential equation is obtained:

$$\frac{\partial^2}{\partial t^2} u_{cr} + \frac{2L_m + L_r}{2L_m L_r C_r} u_{cr} = \frac{1}{L_r C_r}\left(V_d + \frac{L_r}{2L_m} E_{LL}\right)$$

u_{cr}, the bus voltage, is the solution of the differential equation above. Assuming that the bus voltage is zero at the start of the switching cycle, u_{cr} is of the form:

$$u_{cr} = K(1 - \cos\omega_r t)$$

with

$$\omega_r = \sqrt{\frac{2L_m + L_r}{2L_r L_m C_r}}$$

The link frequency is determined by the reactive elements L_m, L_r and C_r. Knowing the load inductance L_m, L_r and C_r is chosen to obtain the desired link frequency.

In cases where $L_L \gg L_r$, ω_r is solely determined by the choice of L_r and C_r and the link angular frequency becomes:

$$\omega_r = \sqrt{\frac{1}{L_r C_r}}$$

5.2. Inverter control

For drive applications, current control is of primary importance. In hard-switched cases, widespread current control techniques are the hysterisis control or PWM current control. One of the features of these techniques is that the switching frequency is not set, but depends on the rate of change of reference and actual currents (or position of the actual current with reference to the hysterisis band). Each of the upper switches is on for 120° following the sequence described in *fig 12* . It remains on during that entire time. After 120° current is commutated in the next upper switch.

The lower switches are also active for 120°, but are pulse width modulated. They are turned on and off as the load current tries to follow the reference. As a lower switch is turned off, load current commutates in the upper diode of the same phase leg.

Current in the soft-switched inverter is controlled based on the same principle. But turn-on and off of the lower switches does not occur randomly, but at selected time intervals that are tied with the link frequency. Switching has to occur only when the bus voltage is zero and this implies that the link frequency must be an integer multiple of the switching frequency. The control circuit should contain an element that enables change of status of switches only when the bus voltage is zero. This element can be implemented by a Zero-Order-Hold. This type of control belongs to the family of Delta Modulators and is called Current Regulated Delta Modulator.

A seven switch is included in the design of this converter. It is operated at the link frequency and shorts the bus for a small fraction of time after the bus voltage has reached zero, thus allowing charging of the resonant inductor. This is significant since the resonant energy must have sufficient energy at the link period to force the capacitor voltage back to zero at the end of the period.
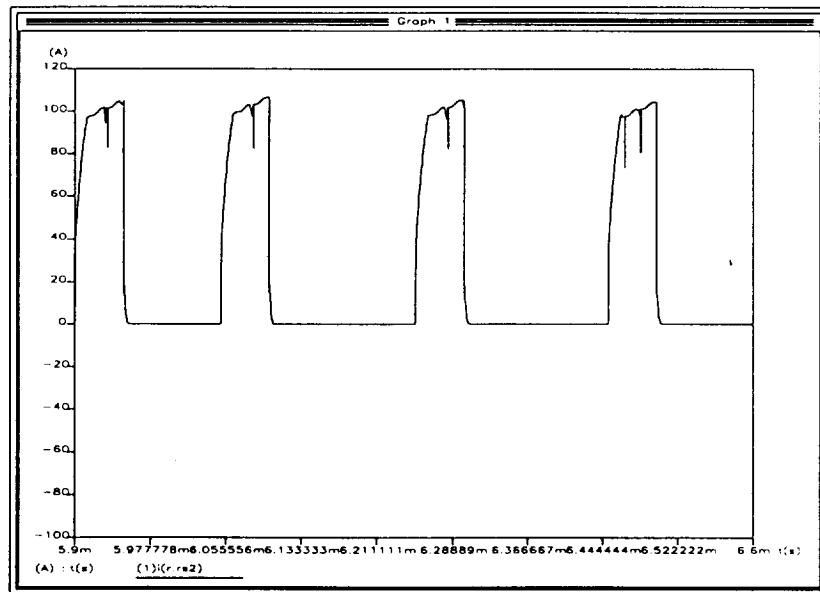
A hard-switched and a soft-switched inverter model for brushless DC were simulated on SABER for comparison of the waveforms. Results are shown in *fig 14-21*.

Switching in the hard-switched case occurs at the full bus or link voltage *(fig 16 & 17)* . During the switching time there are simultaneously high currents and high voltage in and across the switch, thus generating high losses. To keep switching losses low, the switching frequency should be kept below a certain limit.

In the soft-switched inverter, turn-on occurs at zero voltage and is therefore lossless *(fig 14 & 15)* . Switch voltage is not completely zero at turn-off, but the losses generated low if compared to the hard switch case. Another good argument for soft switching is the quasi elimination of recovery effect of the inverter. In hard-switched modes the design of the inverter must take very seriously the recovery behavior into consideration order to avoid damage due to overvoltages caused by high$\frac{\partial i}{\partial t}$. The recovery effect generates additional losses in the diode and in the IGBT.

As explained earlier in the presentation of the soft-switched inverters, the link voltage may peak beyond twice the value of the supply voltage if no clamping technique is used. The peak of the unclamped link voltage is also determined by the amount of energy stored in the inductor when turn-off of a main switch occurs. Control of that energy is done by monitoring the inductor current, at the cost of additional complexity.

Passive clamping is used to limit the capacitor peak voltage under twice the supply voltage. This is particularly clear in *fig 15* where the first oscillation after turn-off of the transistor has a higher peak voltage, only limited by passive clamping. Load current freewheels through a switch and a diode, the load is disconnected from the input and the total input current is pumped into the capacitor causing the higher peak.The clamping ratio has an effect on the link frequency [3].
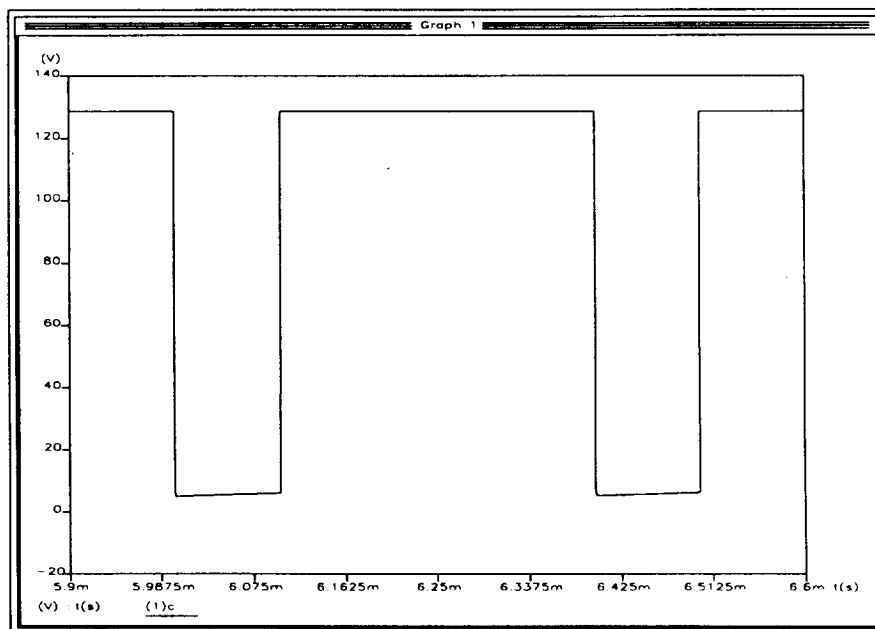
Fig 14 . Switch current for soft-switched inverter
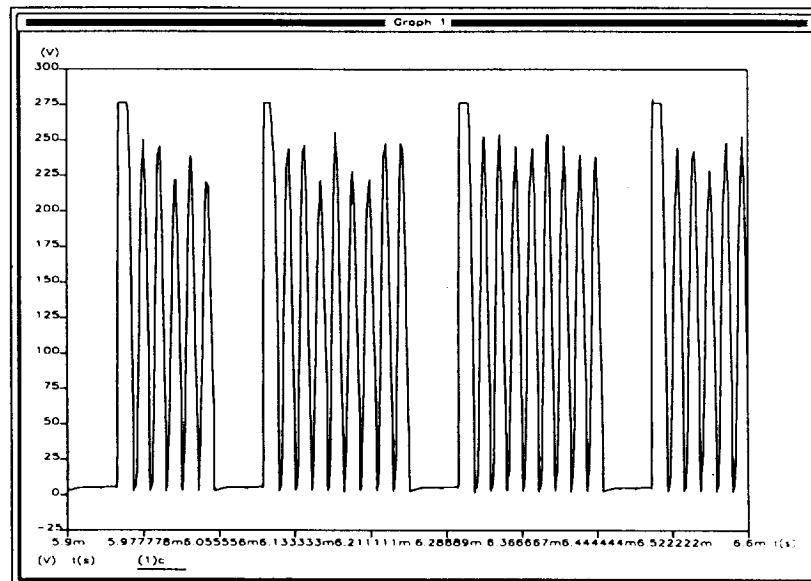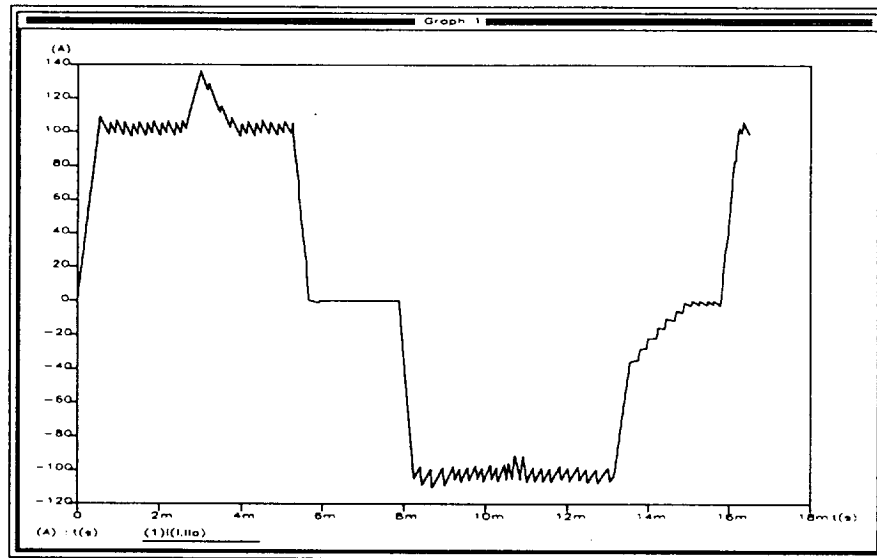

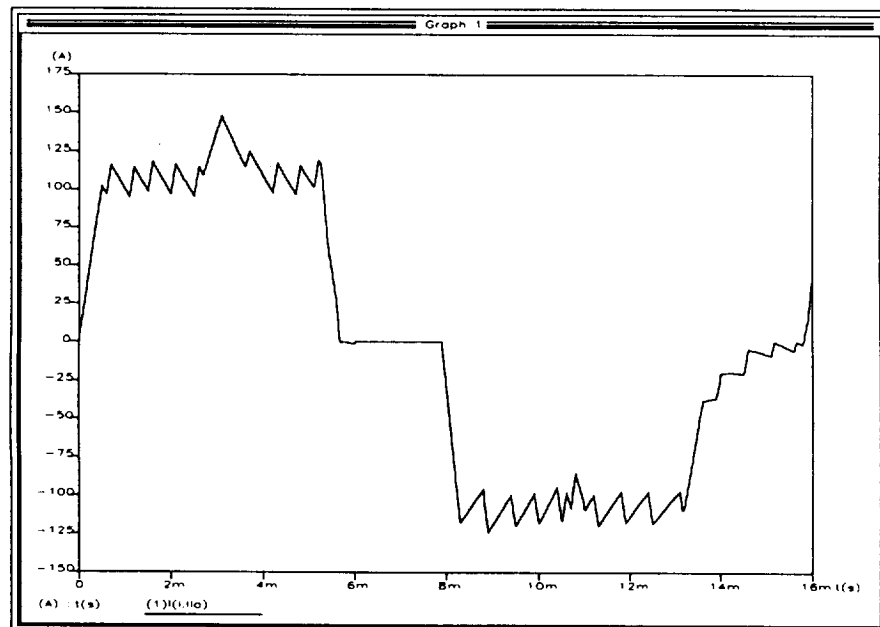*Fig 15 . Voltage across switch for soft-switched inverter*
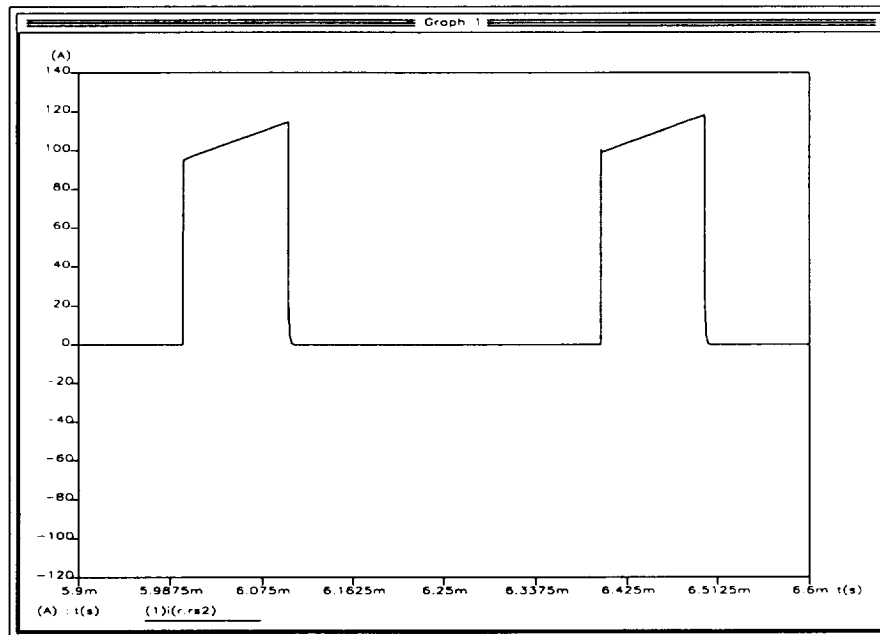
Fig 16 . Switch current for hard-switched inverter
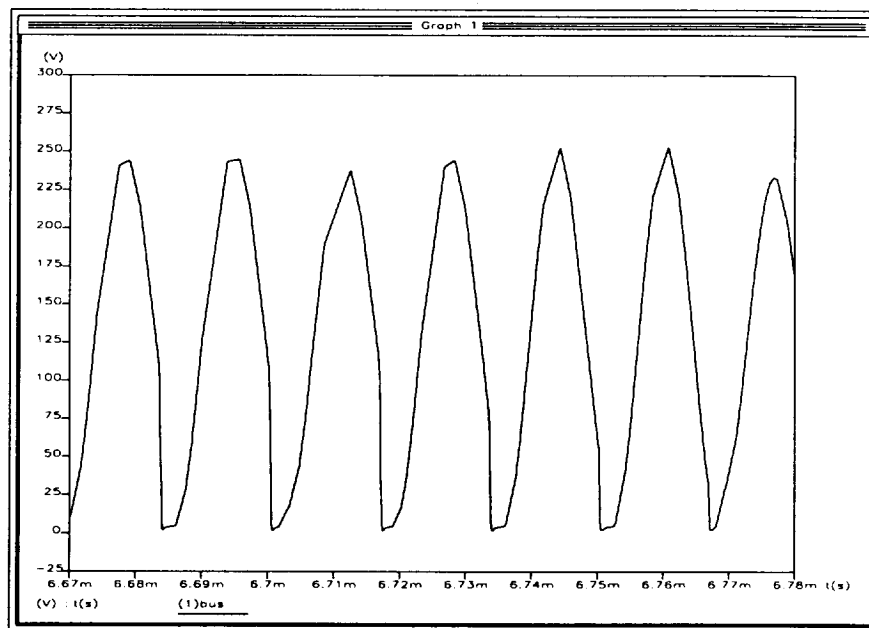

Fig 17 . Voltage across switch (hard-switched inverter)

Fig 18 . Phase current (soft-switched inverter)

Fig 19 . Phase current (hard-switched inverter)

Fig 20 . Link voltage (soft-switched)
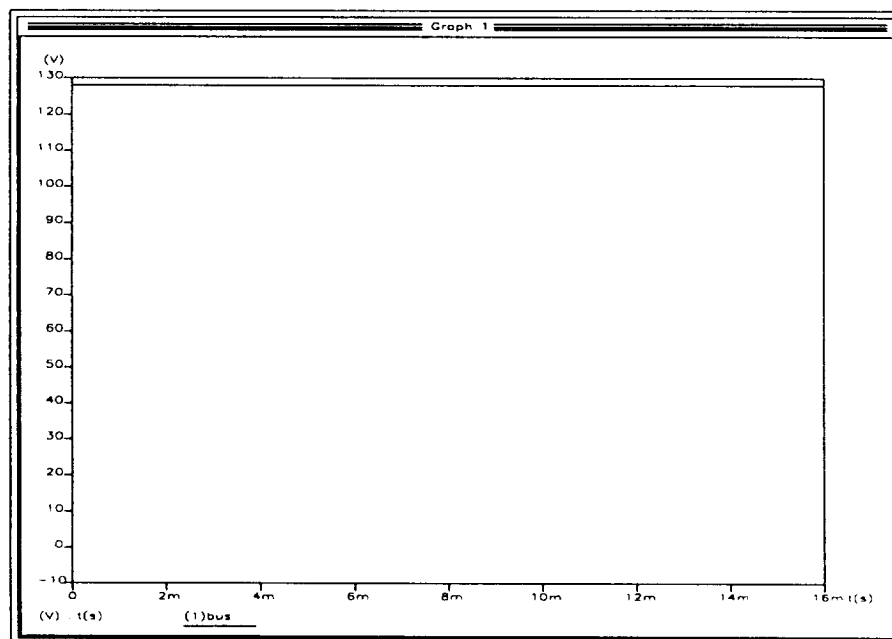
Fig 21 . Link voltage (hard-switched)

6. Losses and Efficiency Calculation

6.1. Losses in the hard-switched inverter

Overall losses in the inverter are the sum of switching losses, conduction losses and recovery losses. An IGBT is assumed for purposes of losses calculation.

6.1.1. Conduction losses
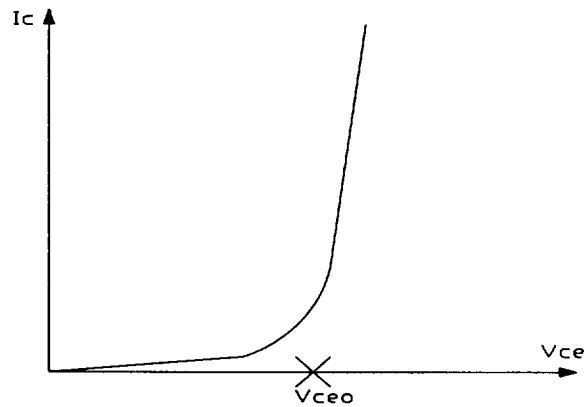
Fig 22 . V-I Characteristics of a transistor/diode

Fig 22 shows the typical voltage-current characteristics of an IGBT/diode, that can be approximated by the linear equation

$$v_{CE} = r_{on} i_C + V_{CEO}$$

where VCEO represents the threshold voltage of the IGBT/diode and r_{on} its on-resistance. v_{CE} is the anode-cathode or collector-emitter voltage. Knowing the current flowing in the device, the power dissipation is calculated by the following:

$$P_f = \frac{1}{T} \int_t^{t+T} v_{CE} * i_C dt = \frac{1}{T} \int_t^{t+T} (r_{on} i_C^2 + i_C V_{CEO}) dt = r_{on} I_{C(rms)}^2 + V_{CEO} I_{C(avg)}$$

The conduction losses in any diode or switch are a function of the magnitude and waveform of the current, since they determine average and rms values of the current flowing in the device.

In switching circuits, conduction losses are produced only when the device is actually on. This notion is expressed in terms of duty cycle, which is the ratio of the on-time of the device (when it conducts current) to the period. Considering the duty cycle δ, the equation becomes

$$P_f = \delta (r_{on} I_{C(rms)}^2 + V_{CEO} I_{C(avg)})$$

For a brushless DC motor with trapezoidal back-emf, the ideal phase current consists of square wave of 120° with a 60° dead time between the positive and the negative current blocks. Current can thus be considered constant for 120°. This corresponds to a duty cycle of 1/3. In the equation above δ can be set to 1/3.

The lower switches are under current PWM or hysterisis control. With the switch on, the input voltage is applied across the series connection of the 2 active phases. When the switch is off current freewheels through the upper diode of the same phase leg and there is no voltage across the 2 active motor phases. Thus current takes less time to rise than it takes to fall since a higher voltage is applied across the load when the transistor is on. It will be assumed that current flows as twice as long in the freewheeling diodes than it does in the lower switches. With the realistic assumption that the switching time (turn-on and off) accounts for 5% of a switching cycle, a real conduction time factor ζ can be defined and set to 95%. (This does not apply for the upper transistors since their switching frequency is low).

$$P_f = \chi \delta \zeta (r_{on} I_{C(rms)}^2 + V_{CEO} I_{C(avg)})$$

$$\chi = 1/3 \qquad \text{for transistor}$$

$$\chi = 2/3 \qquad \text{for diode}$$

6.1.2. Switching losses

The upper transistors turn on and off only once per output cycle. They are operated at the much lower switching frequency and their switching losses can be neglected.

Load current is actually controlled by turn-on and turn-off of the lower transistors. They are under Current Regulated Delta Modulation and are operated at high frequency. High frequency is desired for a better dynamics of the control and minimization of harmonics, but it also generates high switching losses. The graph on the next page represents switching waveforms the derivations are based on.
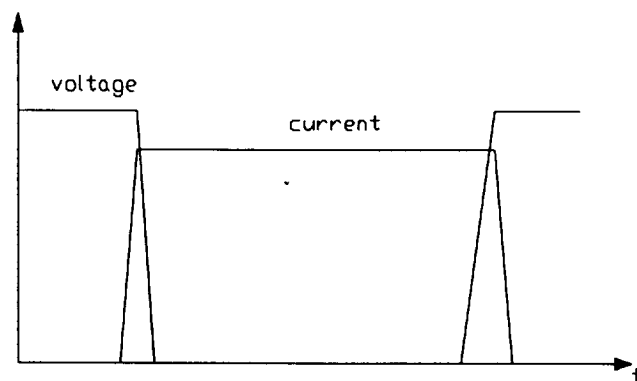
Fig 23 . Switching waveforms for loss calculation

6.1.2.1. Turn-on Losses

Turn-on losses in the lower transistors are determined by the average energy dissipated in the device during turn-on. Assuming a linear rise of current from zero to maximum, energy loss during turn-on is given by

$$e_{on} = \int_{0}^{t_r} V_{bus} \frac{i_C}{t_r} t\, dt = \tfrac{1}{2} V_{bus} t_{rN} \frac{i_C^2}{I_{CN}}$$

t_{rN} and I_{CN} represent rated rise time and rated current as specified in data sheets by the device manufacturer [7].

The device is active for 120° degree (1/3 of output period) and the load current i_c is assumed constant at the value I_L. The average energy loss of an IGBT is

$$E_{on(avg)} = \tfrac{1}{6} V_{bus} t_{rN} \frac{I_L^2}{I_{CN}}$$

and the turn-on losses

$$P_{on} = \tfrac{1}{6} V_{bus} t_{rN} \frac{I_L^2}{I_{CN}} f_s$$

where f_s is an average switching frequency. For a carrier wave PWM control, the average switching frequency f_s is equal to the carrier frequency. In the case of current controlled PWM or hysterisis control, there is no fixed switching frequency. An average switching frequency must be determined.

6.1.2.2. Turn-off losses

The turn-off time of IGBT does not change much with current [7] . The initial rate of current decay very fast. However when the current reaches a certain limit, it decreases logarithmically (tail current). The predominant turn-off time is due to this current tail characteristics [7]. The fall time of an IGBT can be approximated with the function

$$t_f \approx \left(\frac{2}{3} + \frac{1}{3} \frac{i_C}{I_{CN}} \right) t_{fN}$$

where I_{CN} and t_{fN} represent rated current and fall time as specified in data sheets by device manufacturers.

The turn-off energy can then be approximated to

$$e_{off} = \frac{1}{2} V_{bus} i_c t_f$$

The average turn-off energy is

$$E_{off} = \frac{1}{6} V_{bus} I_{CM} \left(\frac{2}{3} + \frac{1}{3} \frac{I_{CM}}{I_{CN}} \right) t_{fN}$$

and the turn-off losses

$$P_{off} = \left(\frac{1}{9} + \frac{1}{18} \frac{I_L}{I_{CN}} \right) I_L V_{bus} t_{fN} f_s$$

6.1.3. Recovery losses

In hard-switched inverters, the recovery of the diodes generates high losses. Those losses can not be neglected for the frequency range of usual hard-switched inverters. At turn-on of the transistor, the recovery effect produces losses in the diode, in the transistor. Furthermore it causes voltage peaks caused by high *di/dt*. The recovery losses for a transistor/diode pair is approximated to:

$$P_{rr} = V_{bus} f_s \left(.416 Q_{rrN} + .305 I_L t_{rrN} \right)$$

where t_{rrN} and Q_{rrN} are the rated recovery time and rated recovery charge [7]. The equation include losses dissipated in both the diode and the transistor by the recovery effect alone.

6.2. Losses in the soft-switched inverter

Soft-switched inverters are developed to realize higher performance and higher power density. Higher switching frequencies are achieved at reduced overall losses. It main drawback is the added complexity to the system. A decision for or against soft-switching is always a trade-off between complexity in the control and reduction of losses. Other advantages of soft-switching such as small size of filter elements might as well be taken into consideration.

6.2.1. Switching losses

Turn-on of the main devices occurs when the bus is shorted. The bus voltage is zero and turn-on is lossless. The important differences compared with hard-switching are the elimination of RBSOA (safe operating area) constraints permitting higher reverse-base currents and smaller storage time. No dynamic saturation exits at device turn-on with the diode conducting. The higher peak voltage and current stresses resulting from diode recovery are no longer relevant.

Turn-off does not occurs at exactly zero voltage. Some losses are produced during turn-off. The resonant capacitor is chosen as to operate in the oversnubbed mode, e.g. the device current reaches zero before the voltage across it has reached its clamping level.

As in the hard-switched case, switching losses of the upper transistors can be neglected since their operating frequency is low.

The lower transistor current at turn-off can be approximated to

$$i_S = I_L\left(1 - \frac{t}{t_f}\right)$$

The current that is turned off is pumped into the link capacitor and rise according to

$$i_{cr} = I_L \frac{t}{t_f}$$

The capacitor voltage thus becomes

$$cr = \frac{I_L t^2}{2C_r t_f}$$

The resonant capacitor is connected across the bus and across the transistor being turned off. Voltage across that device is given by the capacitor voltage.

Dissipation in the device can thus be found to

$$P_d = V_{cr} i_S = \frac{I_L^2}{2C_r t_f} t^2 \left(1 - \frac{t}{t_f}\right)$$

Turn-off losses for a lower transistor can then be approximated by multiplying the turn-off energy by $f/3$ since it is active for only $1/3$ of the output period.

Switching does not always occurs after each sampling period since it also depends on the difference between actual and reference current. The switching frequency is actually less than the sample frequency. The instantaneous device dissipation has at $t=2t_f/3$ the maximum value.

$$P_{dm} = \frac{2I_L^2 t_f}{27 C_r}$$

and the average device switching losses for an average frequency f_s are [5]

$$P_{off} = \frac{I_L^2 t_f^2}{24 C_r} f_s$$

The fall time t_f defined here is considerably smaller than in the hard-switched case.

6.2.2. Conduction losses

Higher switching frequency is the main reason behind the selection of a soft-switched inverter. But higher switching frequency does have only a slight effect on the losses of the higher transistors compared to the hard-switched case. The main reason is that their mode of operation does not change. For same current conditions, those losses can be assumed equal in both cases.

The lower transistors are controlled by Current Regulated Discrete Pulse Modulation and are considerably affected by the increase in switching frequency. Higher switching frequency means more switching time and less conduction time. The duty cycle of the lower transistors and the freewheeling diodes is therefore reduced by a factor with respect to the hard switched case. By realistically assuming that switching time is about 5% of a switching period, a four times increase in switching frequency causes the previously defined real conduction time factor ζ to reduce to 80% during the active phase. This factor is included in the conduction losses calculation for the soft-switched inverter as compared to a factor of 95% for the hard-switched inverter.

It is basically possible to obtain the losses by SABER or Pspice simulation. But those software package do not simulate at the present the recovery effect of fast diodes. Given the

importance of the recovery of diodes in hard-switched inverters, the results will be inaccurate.

Losses and efficiency calculations are therefore based on the equations given in the previous sections.

6.3. Efficiency Calculations

In quiescent state the motor must deliver 40 hp. This requires a phase current magnitude of about 250 A for the brushless DC motor. The motor drive should also be able to peak at 110 hp, which corresponds to a current of about 650 A.

Here are the specifications of the inverters used in the losses and efficiency calculation. Switching frequencies are average values.

	Hard-switched	Soft-switched
Input voltage	128 V	128 V
Phase current	250 - 650 A (square)	250 - 650 A (square)
Output frequency	63.33 Hz	63.33 Hz
Switching frequency	5 kHz	20 kHz
Link frequency	-	60 kHz
Resonant inductor L_r	-	12.75 uH
Resonant capacitor C_r	-	500 nF

Table 4 . Inverter specifications

The data of part 1MBI300L-120 of Fuji are used in order to evaluate the losses in a real environment. Part 1MBI300L-120 is an IGBT modul with the following data:

	Value	Units
Collector-Emitter voltage	1200	V
continuous current	300	A
Peak current	600	A
Transistor threshold voltage V_{CEO}	2.2	V
Diode threshold voltage V_F	1.8	V
Transistor on-resistance r_{Ton}	12.5	$m\Omega$
Diode on-resistance r_{Don}	11.5	$m\Omega$
Rise time t_r	.6	μs
Fall time t_f	2.3	μs
Recovery time t_{rr}	.2	μs
Recovery charge Q_{rr}	4400[1]	nC

Table 5 . IGBT 1MBI300L-120 data

Using the formulas derived in previous sections, the inverter losses are calculated for phase currents of 250 A, 350 A and 600 A.

	I_L=250 A	I_L=350 A	I_L=600 A
Cond. loss T1, T3 or T5	443.75 W	802.08 W	1940 W
Cond. loss T4, T6 or T2	140.52 W	254 W	614.34 W
Cond. loss D1, D3 or D5	246.73 W	430.35 W	1102W
Turn-on loss T4, T6 or T2	13.2 W	26.163 W	78 W
Turn-off loss T4, T6 or T2	57.96 W	92 W	196 W
Recovery loss D1, D3 or D5	113.41 W	158.3 W	270.55 W
Total Losses	3046.71 W	5287.63 W	12602.7 W

Table 6 . Losses in the hard-switched inverter

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[1] not given in data sheet

	I_L=250 A	I_L=350 A	I_L=600 A
Cond. loss T1, T3 or T5	443.75 W	802.1 W	1940 W
Cond. loss T4, T6 or T2	118.33 W	213.9 W	517.34 W
Cond. loss D1, D3 or D5	207.77 W	362.4 W	928 W
Turn-on loss T4, T6 or T2	0	0	0
Turn-off loss T4, T6 or T2	26 W	51 W	150 W
Recovery loss D1, D3 or D5	0	0	0
Total Losses	2387.55 W	4288.2 W	10606 W

Table 7. Losses in the soft-switched inverter

The efficiency of an inverter is defined as

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{in} - \Sigma P_{loss}}{P_{in}}$$

The equation above assumes that losses of the inverter are produced only by the active device (transistors and diodes). Losses in the reactive elements (L_r, C_r) and in the wire are neglected. The efficiency of the motor is not considered here since the main focus is on the comparison of soft-switched versus hard-switched inverter.
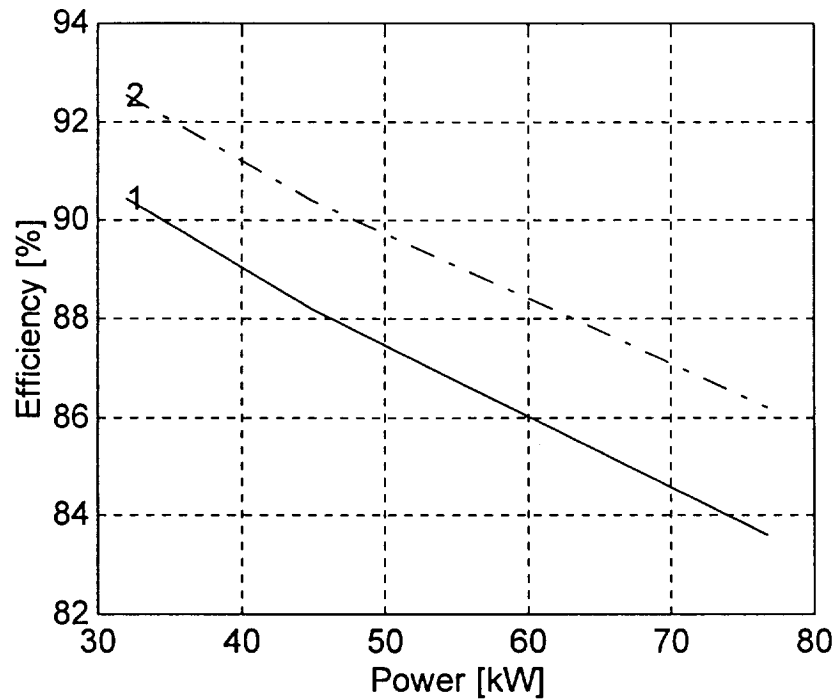
		hard	soft	hard	soft
	P_{in} [kW]	ΣP_{loss} [kW]	ΣP_{loss} [kW]	η [%]	η [%]
$I_L = 250$ A	32	3.05	2.388	90.47	92.54
$I_L = 350$ A	44.8	5.288	4.288	88.19	90.43
$I_L = 600$ A	76.8	12.603	10.6	83.59	86.2

Table 8 . Efficiency

In *fig 24 & 25* , curve 1 shows losses or efficiency for the hard-switched case and curve 2 is for the soft-switched case.
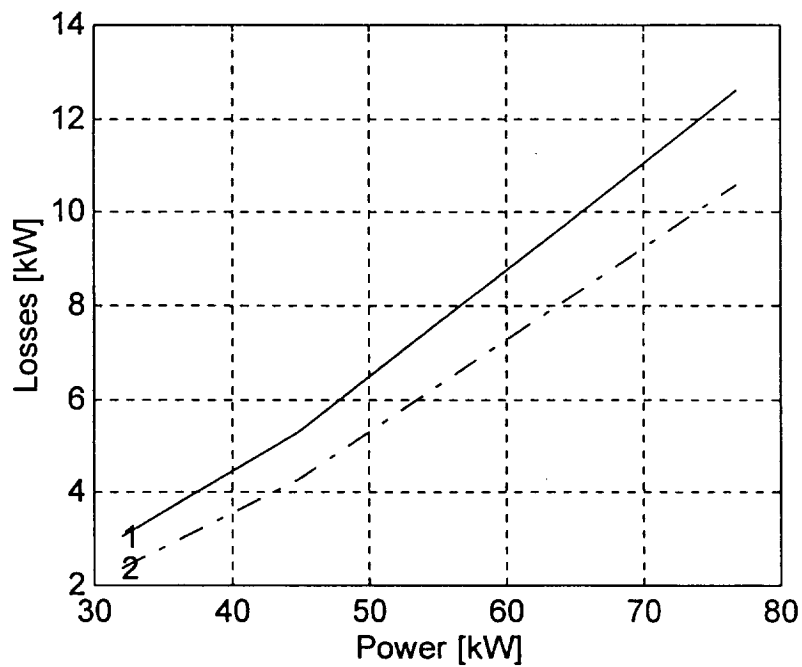
Fig 24 . Inverter losses comparison

Fig 25 . Efficiency comparison

At 20 kHz, the soft-switched inverter still produces less overall losses than the hard-switched inverter operating at 5 kHz . The efficiency of the inverter is improved by an average of 2.5% over the given power range *(fig 25)* . The combination of soft-switched inverter and brushless DC motor can guarantee an overall efficiency of the motor drive over 90% in the range 40-60 hp. Possible load scenario indicates that delivery of power above 60 hp is required only for very short time intervals.

Soft-switching offers many other advantages such as drastic reduction of EMI, small size of filter elements, reduction of audible noise. In addition to meeting the efficiency requirement, the size and weight of the motor drive are reduced. This motor drive is really a strong candidate for this particular space application.

7. Conclusion

This study examines different motor drive candidates for space restricted applications. The conventional three-phase hard-switched inverter and the induction motor are standard in the industry today. The hard-switched inverter is a mature technology and its control is the focus of numerous literature. But space applications have special requirements which demand unconventional solutions. The combination of soft-switched inverter and brushless DC motor is a strong candidate for such an application.

The brushless DC motor has proven to be very efficient and should be a better choice than the standard induction motor due to its better efficiency. In order to achieve optimal results with respect to efficiency, a soft-switched inverter is used to drive the motor. Results have shown that the inverter losses are reduced despite the fact that the soft-switched inverter operates at a much higher frequency, thus improving the motor drive efficiency.

Considering the many other advantages of soft-switching, this motor drive is surely the best candidate among the motors and inverters presented in this study.

Soft-switching is new in the area of inverters and the technology is not yet mature. But a lot of research is being done and the results are promising, making this choice even more attractive for the future.

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